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ISPD Panel: Trends in ASIC Design Flow

From a Tool Vendor Perspective

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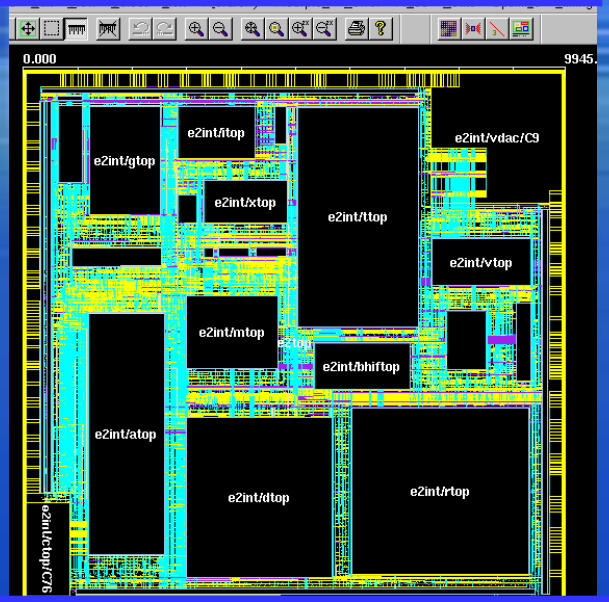
Outline: High End ASIC Design

- Reference point: “typical” design
- Use of hierarchy in design
- Handoff from logic design to physical design
- Physical tie-ins to synthesis
- Noise problems

Typical Q1 2001 ASIC Chip

- **Borderline "SOC"**
  - Video Graphic Chip
  - Network interface/router chip
  - 0.18 u technology, 6 - 8 layers
- **Design**
  - 5 large blocks, each with
    - ~12 RAMS
    - 5K pins
    - 250K instances
    - 5 global clocks, 200 derived/gated clocks
    - *27K lines of timing constraints*
      - set_output_delay 4000 -clock Clk1 -rise -min -add_delay [get_ports {MemWriteBus[3]}
      - set_false_path -setup -rise -from [get_pins {GR_FE_STAGE1_CNTRL_MISC24BIT_REG_1_16A/CK}]
- **Care abouts**
  - Correctness
  - *Timing convergence*
  - *On time delivery*



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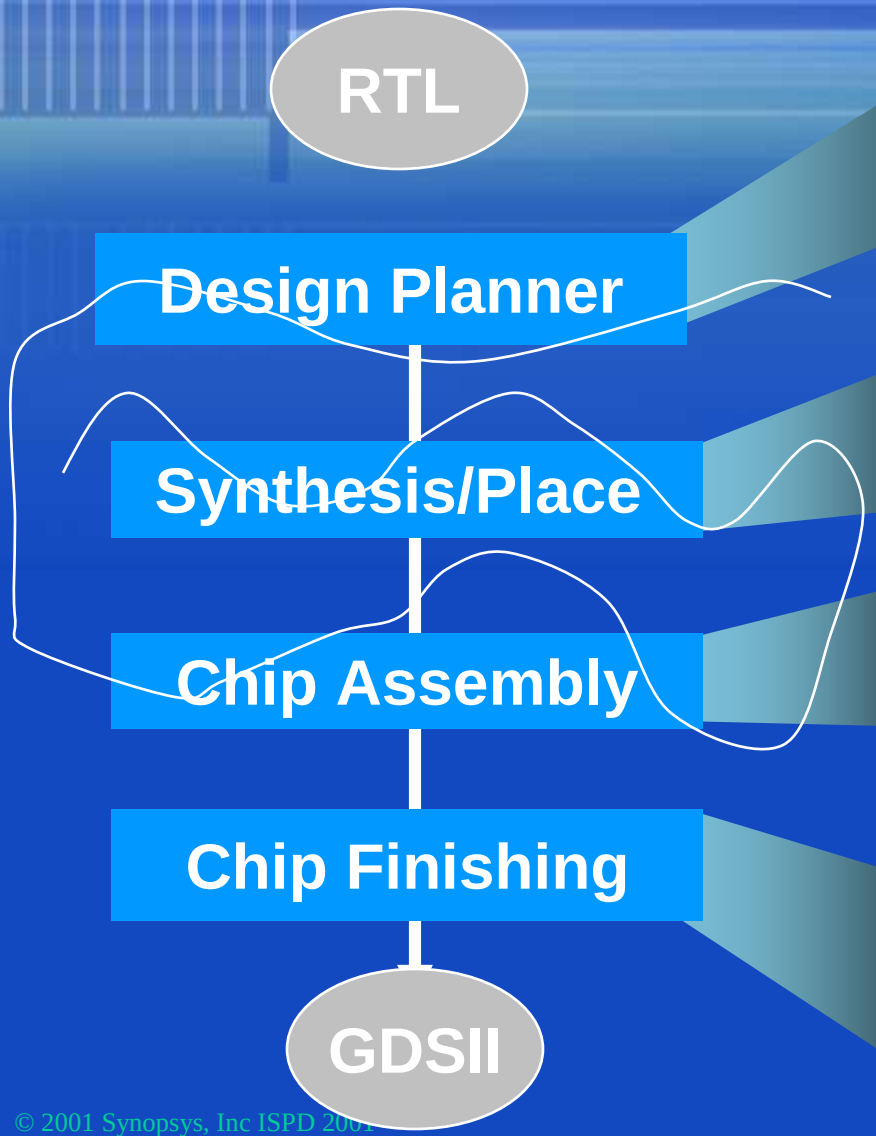
ASIC Flow: Got Hierarchy?

- All chips have hard blocks in them
- Percent of design starts that are hierarchical increases yearly
  - methodology: insulates sub-projects
  - tool reasons: capacity
  - IP reasons: may not have control over some blocks
- In 2001, about 50% of high-end ASIC chips are “hierarchical” and have soft blocks that are placed independently

Logic to Physical Flow (simplified)



Chip RTL Planning
Synthesis1, Floorplan Generation,
Chip Level Time Budgeting

Block Implementation
Synthesis2 & Placement
Block routing

Chip Integration
Chip Timing Closure: Pins,
Buffers, Global Routing

Finalize Top Level Routing,
Extraction,
Address (or ignore)
Signal Integrity Issues, LVS+DRC

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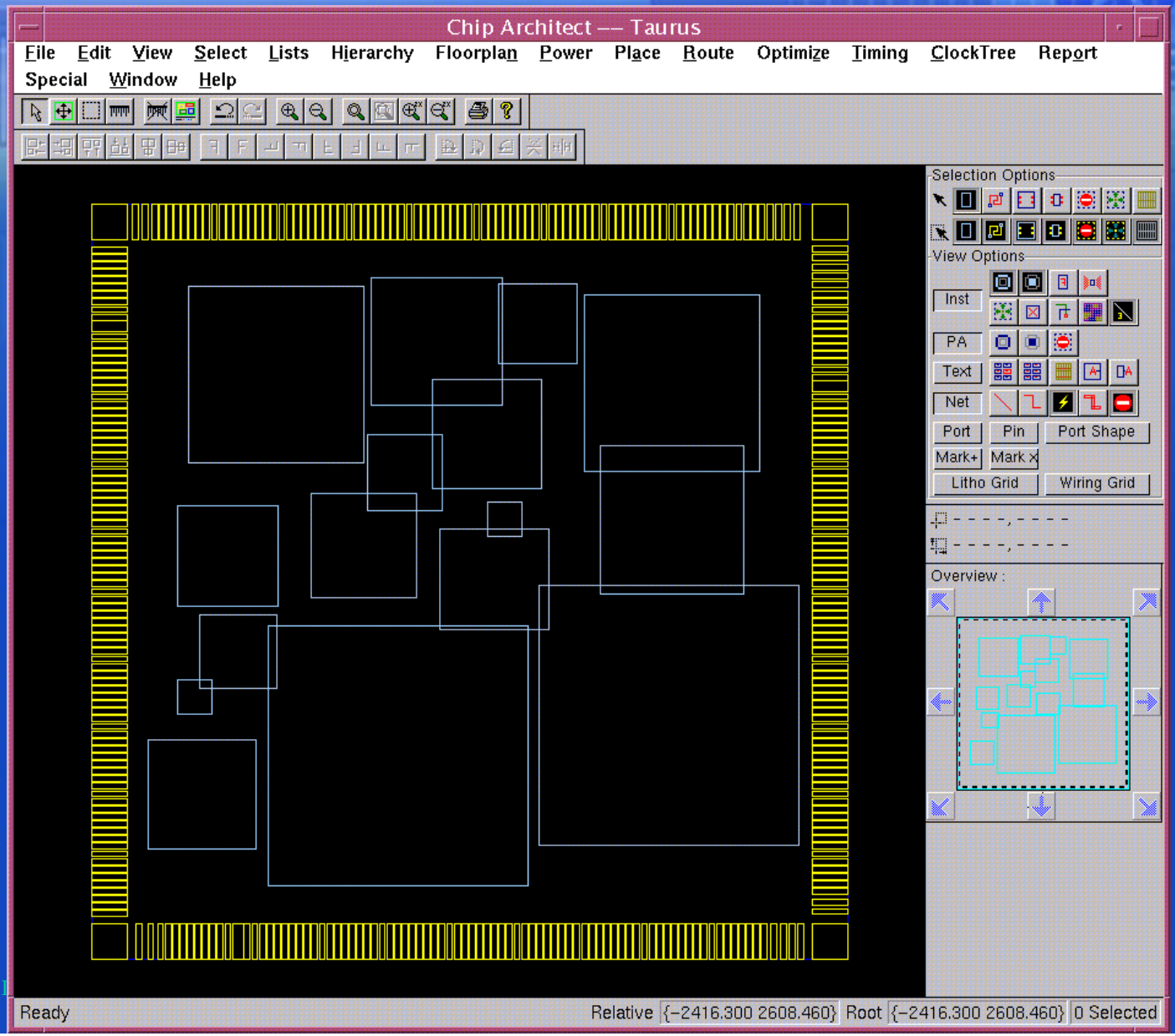
Black Box from Initial RTL model



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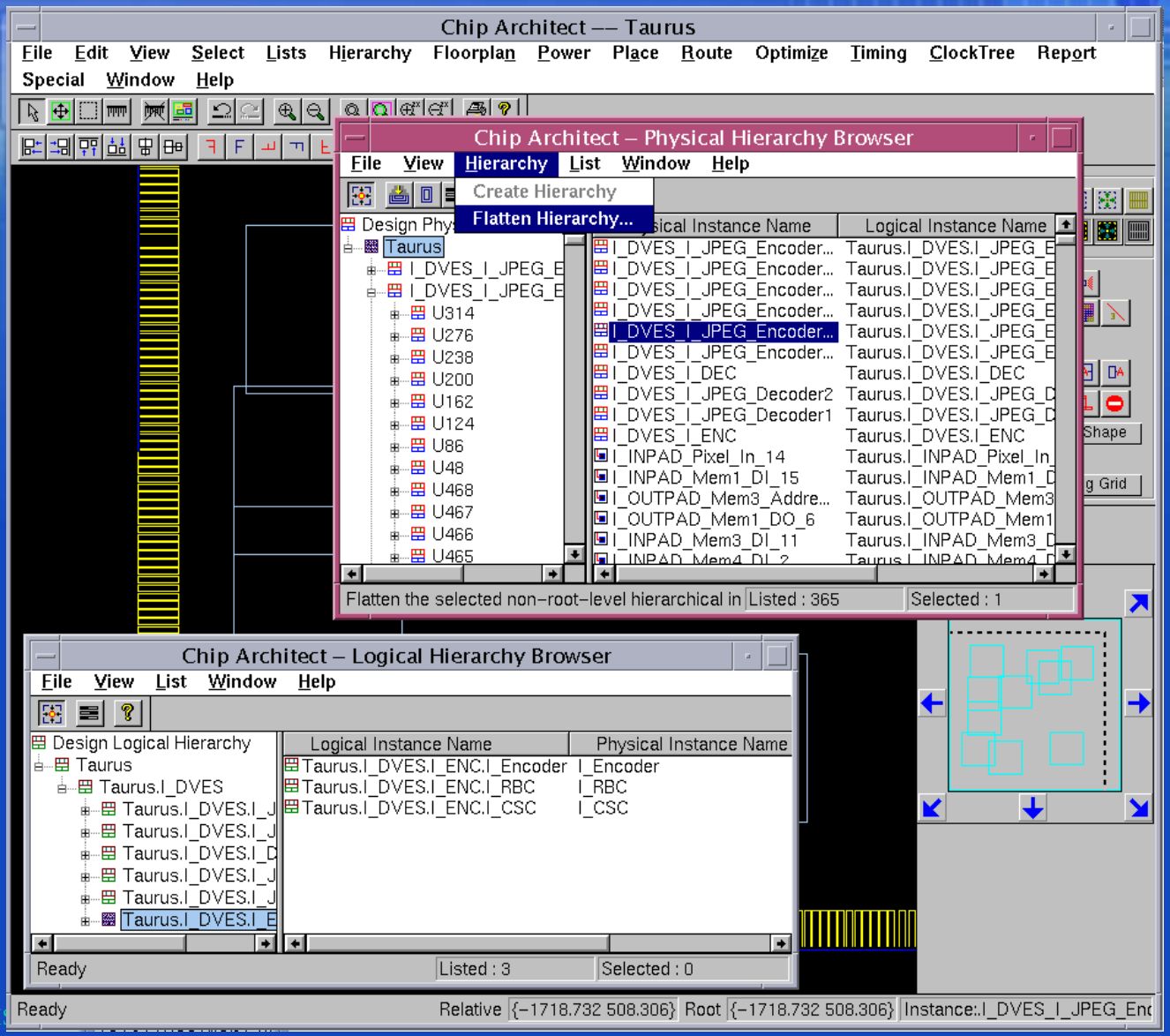
Tying Logical to Physical Blocks



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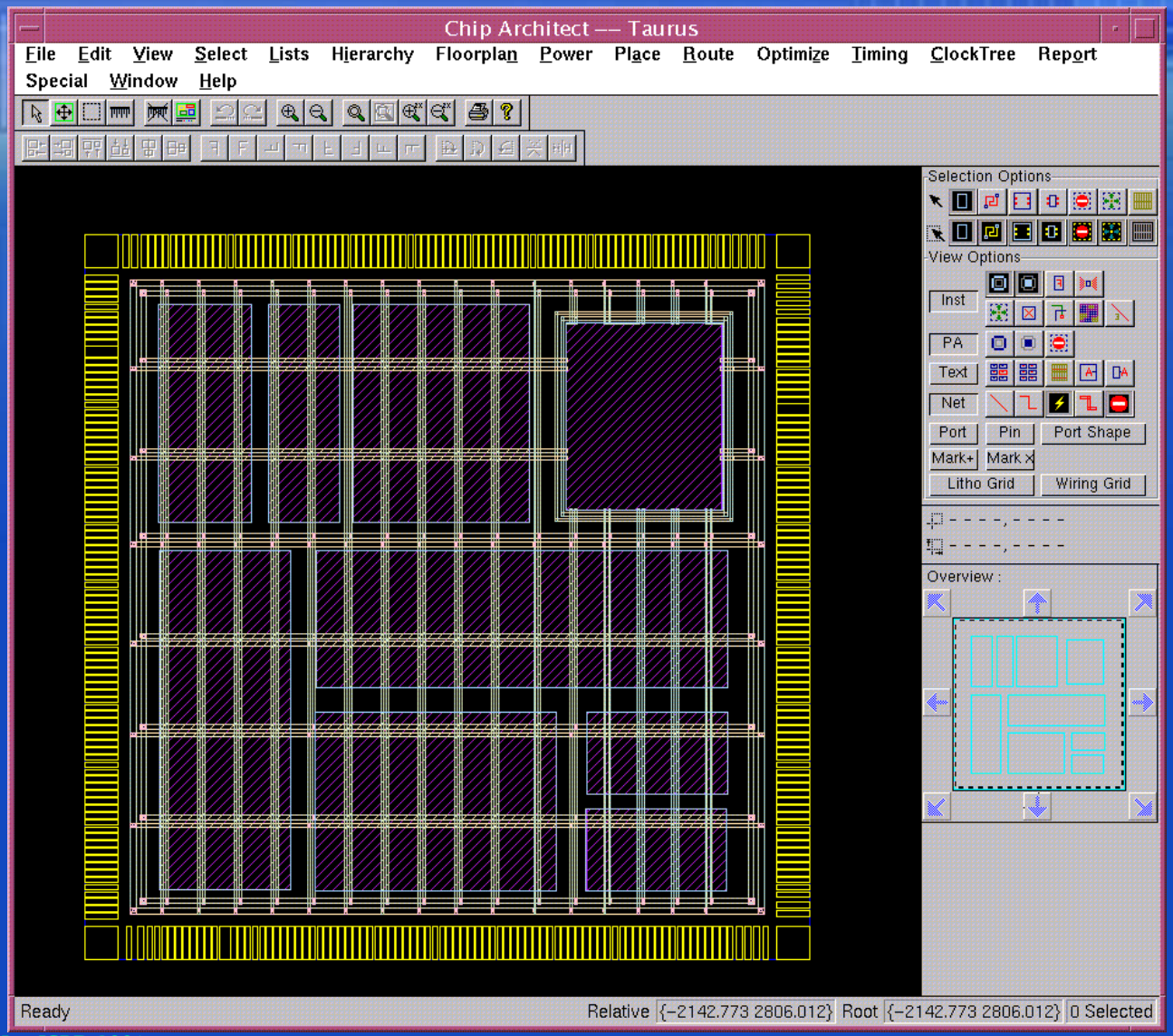
Getting More Physical



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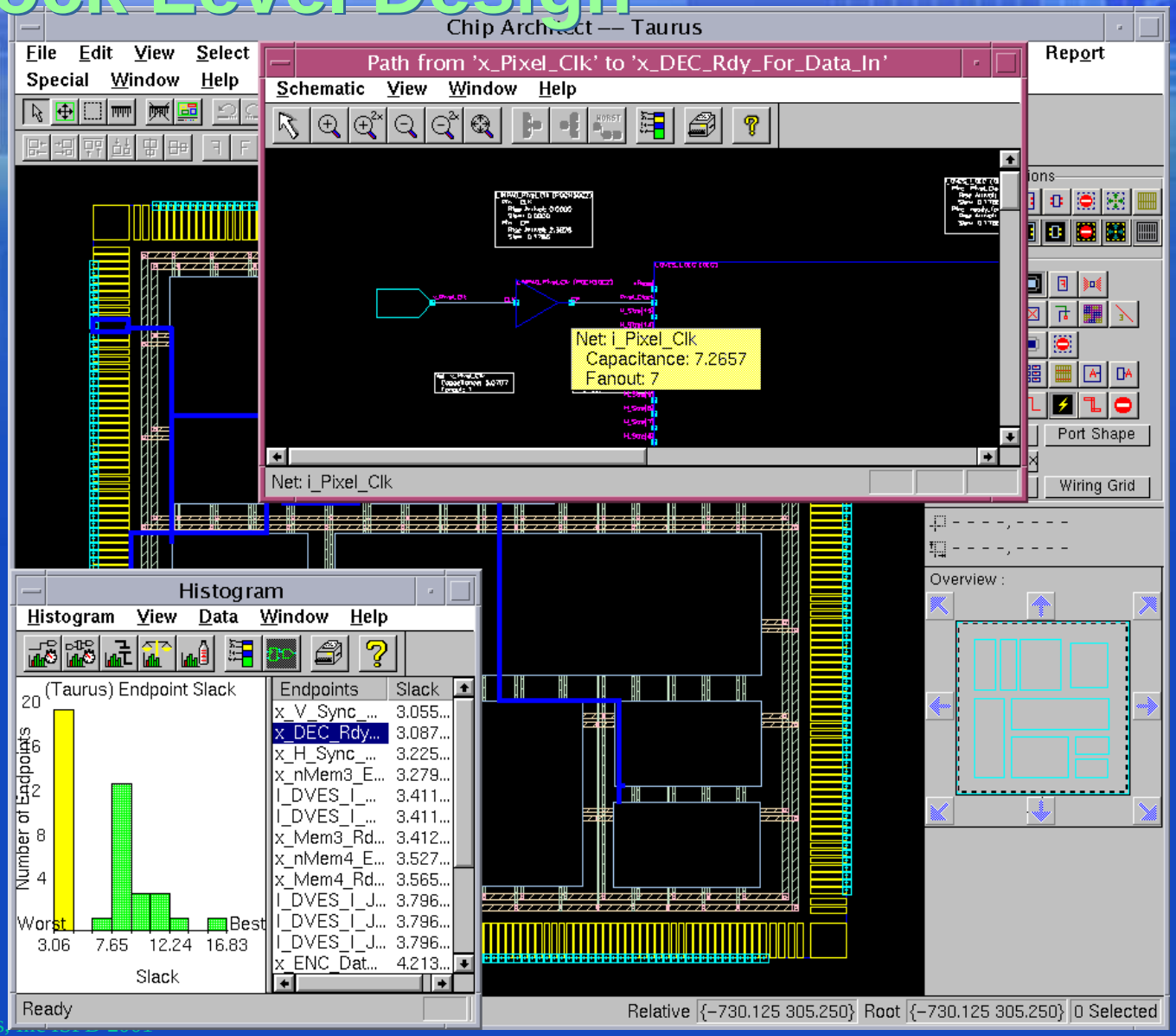
Realistic Timing Numbers after Block Level Design



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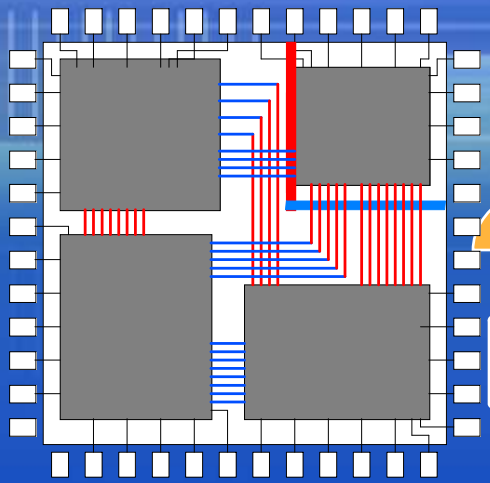
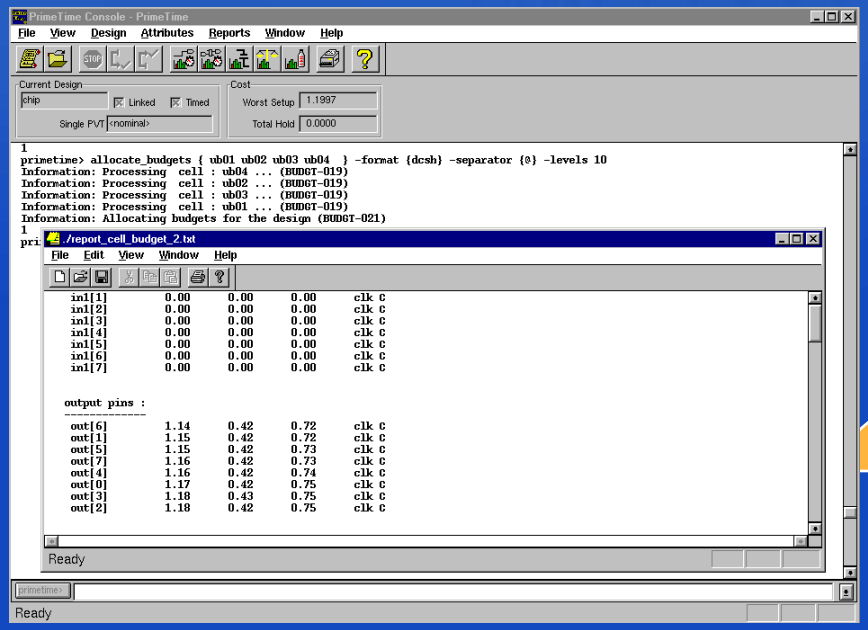
Key to Timing Closure: Time Budgeting

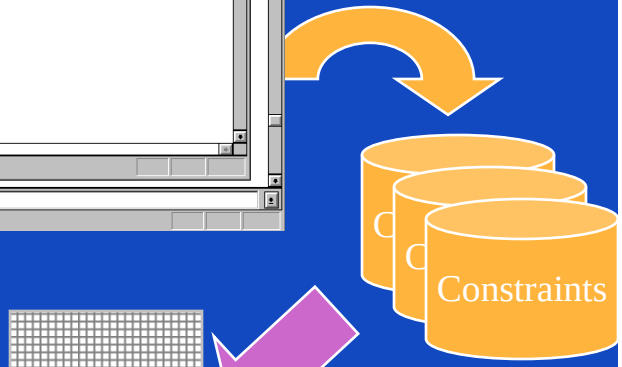


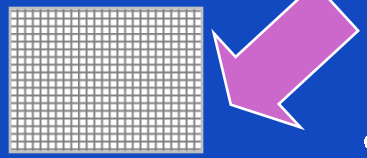
- Applied at many levels: chip, block, path...

Parasitics



Start after entities are identified, not necessarily defined





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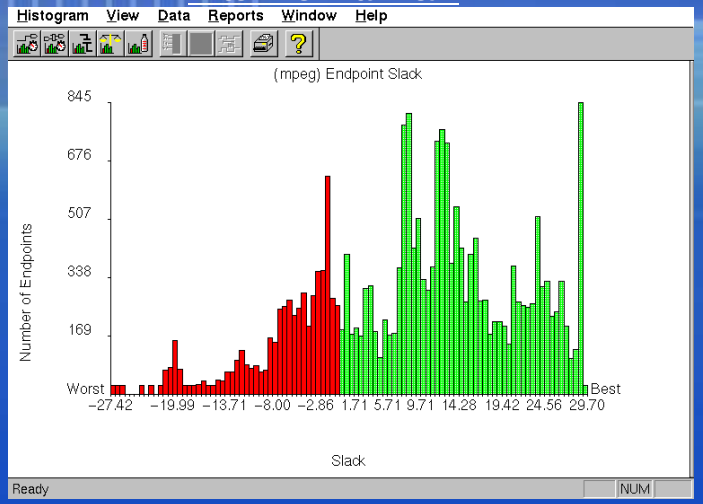
Block Implementation: Core of Physical Synthesis

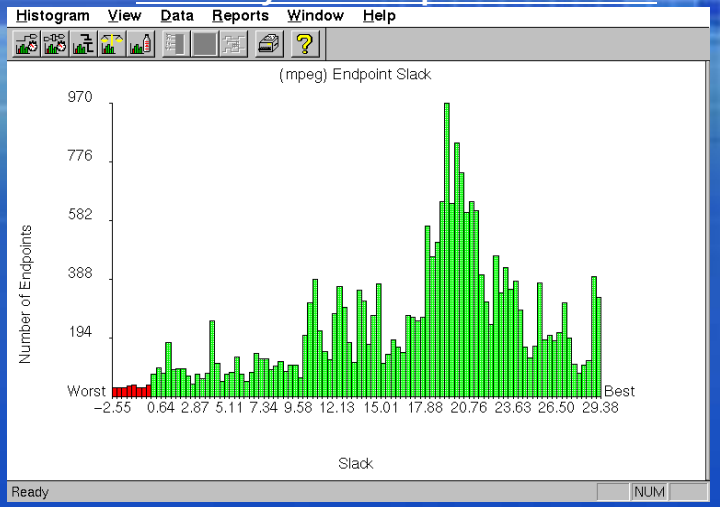
- **Physical Synthesis**
  - turn generic logic gates with no placement into
  - optimized gates with detailed placement
- **Requires context from chip:**
  - shape
  - obstructions
  - pin positions
  - timing constraints, etc

Timing Effect of Physical Synthesis

After Normal P&R



After PhysicalCompiler Placement

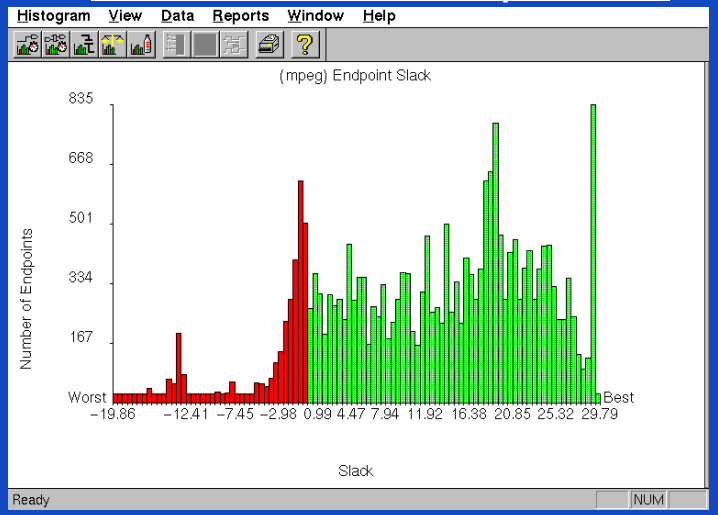


Positive

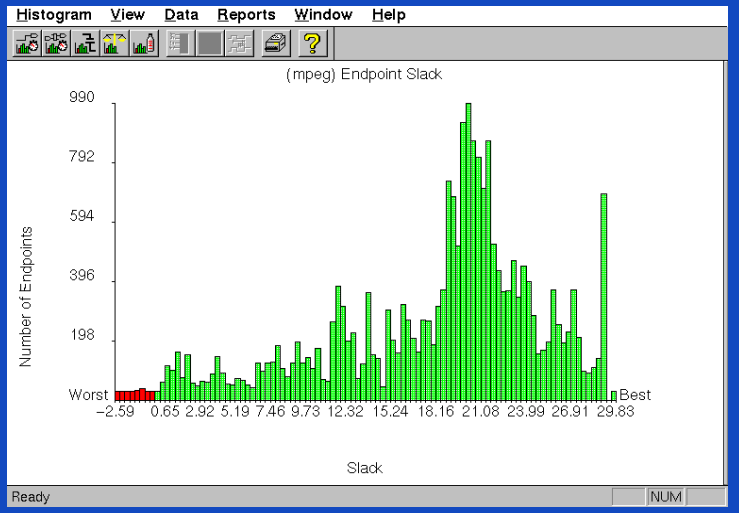
Negative

700K gates
0.25u
10 ns
32 RAMs

After Normal P&R + Post Optimization



After Wroute with PhysicalCompiler Placement



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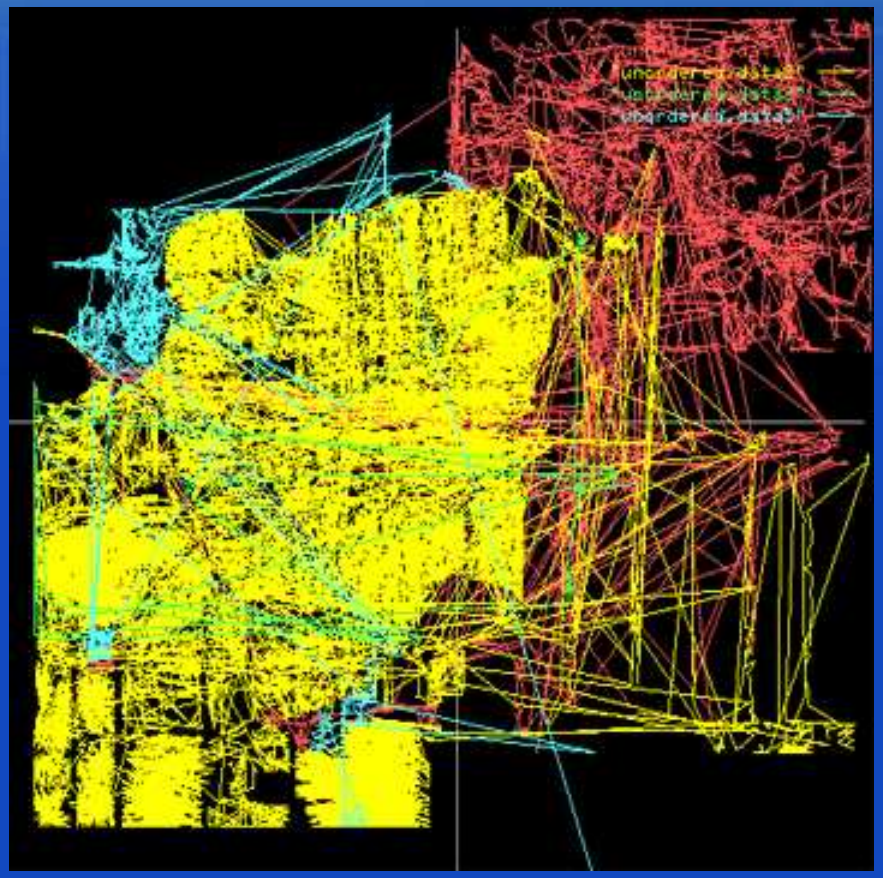
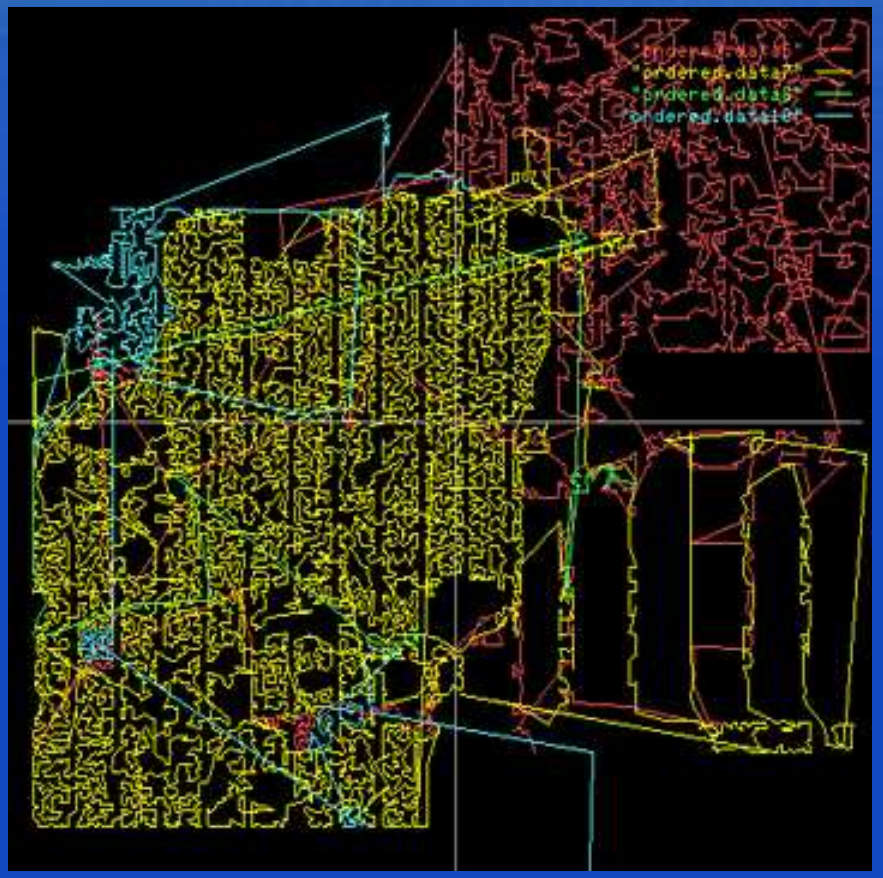
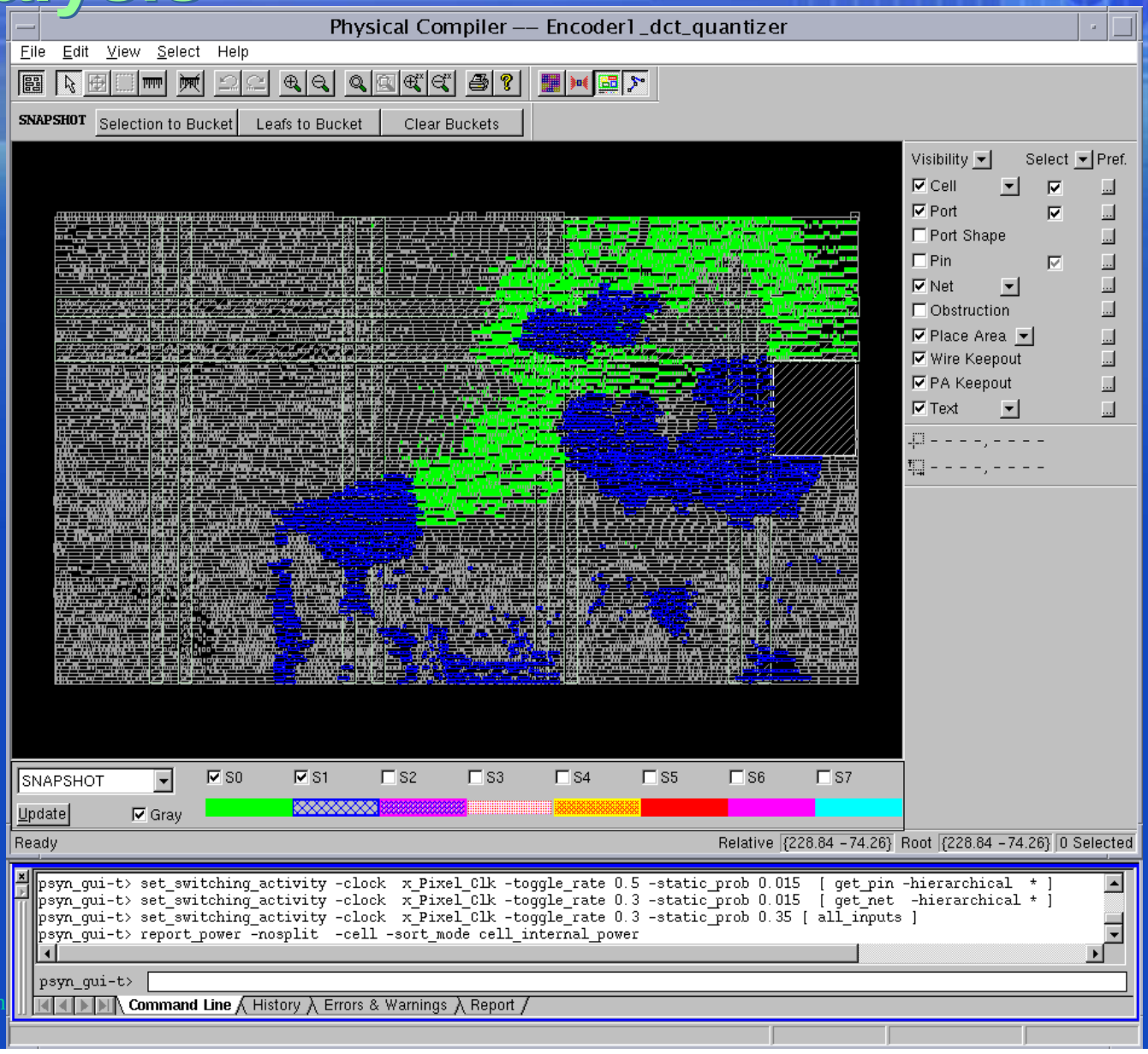
Integration of Physical Synthesis: Linking with Test

Path reordering can be chosen to reduce wiring congestion





Physical Synthesis & Power Analysis



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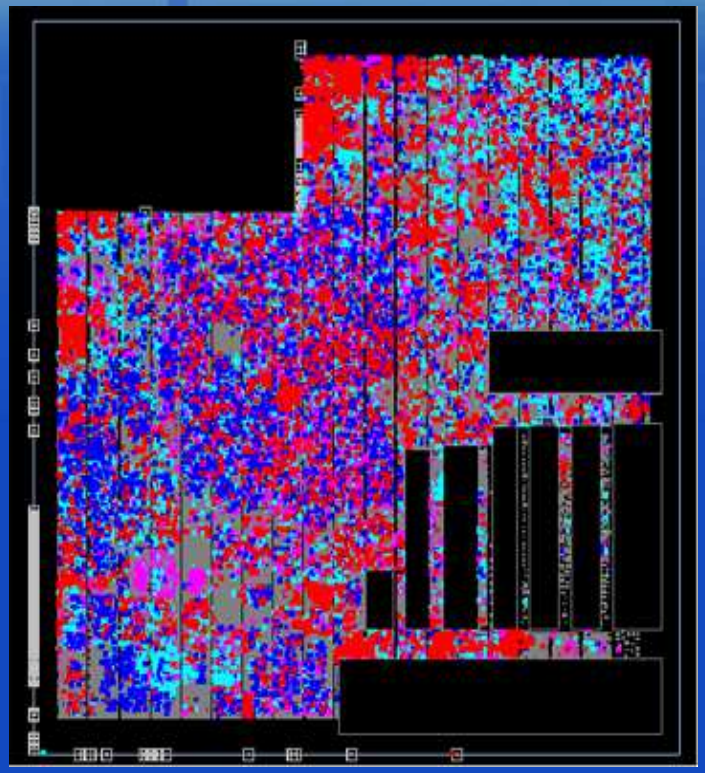
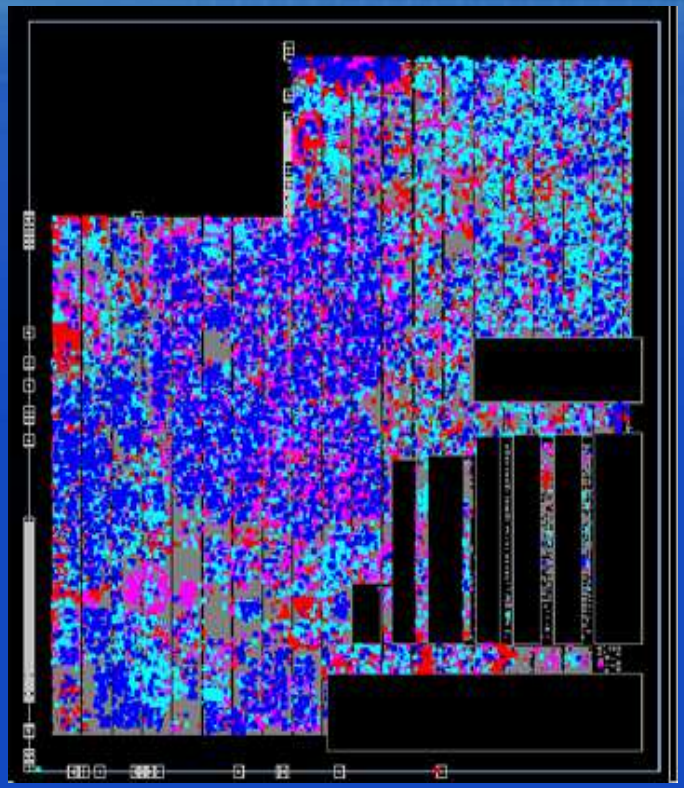
Phy. Synthesis & Power Optimization

- Gates can be resynthesized based on wire length
- Gated clocks can be inserted by proximity

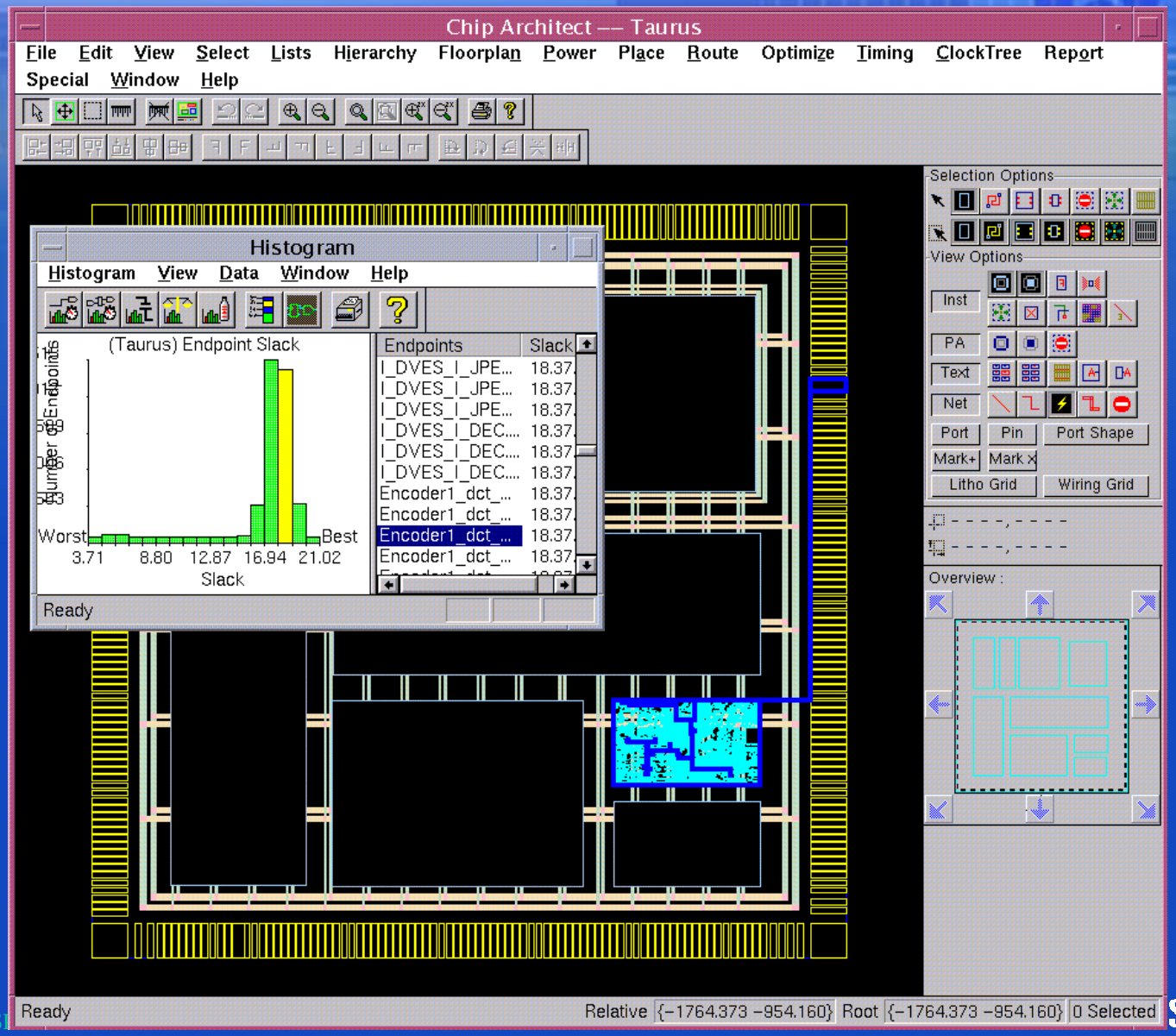


Power Consumed = 2.4W



Power Consumed = 1.2W

Assembly of Blocks into chip



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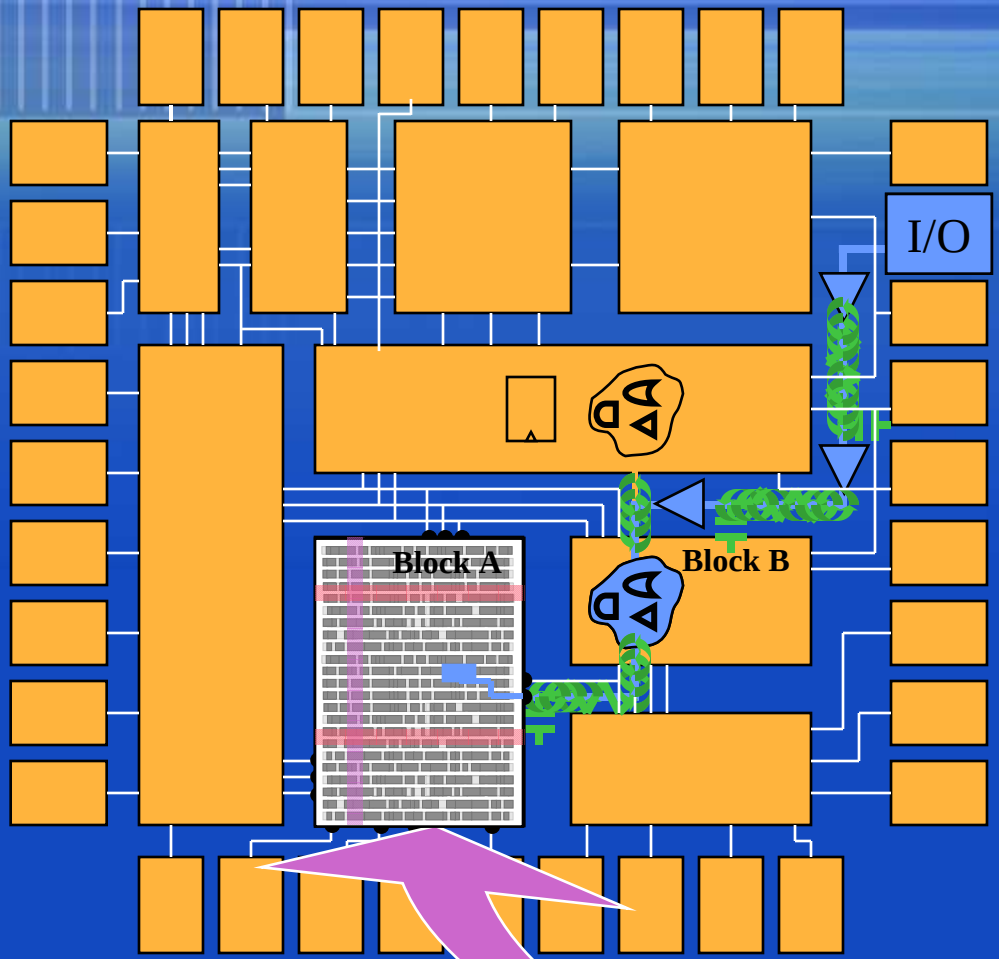
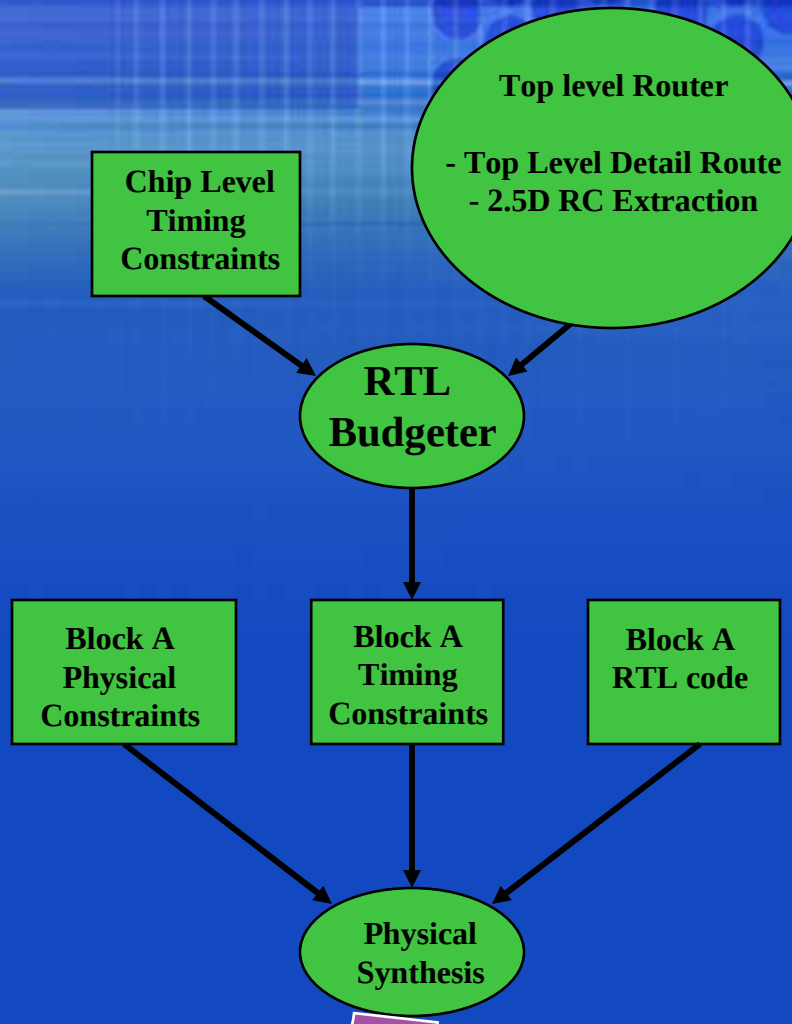
Chip-Level Timing Closure





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Summary: High End ASIC compared to MicroProcessor

- Typical High End design - integration of subsystems, each of which has its own specs. Complexity similar to microprocessor.
- Use of hierarchy in design: required
- Handoff from logic design to physical design: no such thing
- Physical tie-ins to synthesis: several, and growing. But automated, not manual
- Noise problems: ominous, ignored at some peril